PATENT APPLICATION
DOCKET NO.: 200208999-2

REMARKS

Claims 1-36 are presented for examination, of which claims 1, 16, and 27 are in independent form.

No claims have been amended by way of the present response.

Favorable reconsideration of the present application as currently constituted is respectfully requested in light of the arguments herein.

Regarding the Claim Rejections - 35 U.S.C. §102(b)

Claims 1-36 are rejected in the pending Office Action under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,887,003 to Ranson et al. (hereinafter the *Ranson* reference). In connection with these rejections, the Examiner has commented as follows with respect to base claim 1:

> Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the GPPC comprising:
> an AND/OR circuit connected to receive the debug data (col. 12, lines 30-62);
> a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated, causes the counter circuit to increment a current count value (col. 15, lines 56-67 to col. 16, lines 1-39); and
> a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected

block of the debug data having a designated relationship to a compare value (col. 12, lines 30-62; col. 11, lines 9-2 1; col. 15, lines 27-55; col. 19, lines 18-67; col. 20, lines 1-14),

wherein the AND/OR circuit activates the increment signal responsive to one or more selected bits of an events signal being set (col. 15, lines 56-65; col. 16, lines 16-39).

Applicant respectfully traverses the pending §102(b) rejections of the claims as set forth above and offers the following discussion as support. As set forth in base claim 1, an embodiment of the present patent application is directed to a general purpose performance counter connected to a bus carrying debug data. The general purpose performance counter contains, *inter alia*, an AND/OR circuit connected to receive the debug data, wherein the AND/OR circuit activates an increment signal if at least one of the selected bits of an events signal is set.

Similarly, base claim 16 is directed to another embodiment of a general purpose performance counter connected to a bus carrying debug data that contains, *inter alia*, an AND/OR circuit connected to receive the debug data, wherein when the AND/OR circuit is in AND mode, the AND/OR circuit activates an increment signal if all of one or more selected bits of an events signal are set and when the AND/OR circuit is in OR mode, the AND/OR

circuit activates the increment signal if at least one of the selected bits of the events signal is set.

Base claim 27 is directed to an embodiment of a method of implementing a general purpose performance counter connected to a bus carrying debug data. The claimed embodiment involves, *inter alia*, providing an AND/OR circuit connected to receive the debug data and activating an increment signal by the AND/OR circuit responsive to one or more selected bit of an events signal being set.

The *Ranson* reference is directed to a scheme for comparing a group of multi-bit binary fields with a multi-bit expected pattern to generate a set of final match results. For each multi-bit binary field, *Ranson* compares the field with the expected pattern, generates mask results that select the desired portion of the result, and creates preliminary match results equal to a logical ANDing of all bits making up the bitwise mask result. Secondary match results may be generated by negating all of the preliminary match results and final match results are generated by individually gating all of the secondary match results with separate enable indicators. See Abstract. *Ranson* appears to teach that a hit may be indicated only when all of the

selected bits in a binary field are set. To put it differently, no indication of a hit is provided in *Ranson* if fewer than all of the selected bits are set.

These actions are seen most clearly in Figure 12 of *Ranson*, which is discussed in one of the cited passages, column 15, lines 19-55. *Ranson* discloses that the four bits of present state bus 1114 are provided to one of the inputs of comparator 1212 so that they may be compared with the contents of storage element 1201, which specifies the present state during which entry 1200 will become active. The four bits that are output from comparator 1212 are ANDed together by AND gate 1216, yielding a one-bit match result for present state. Similarly, the contents of storage element 1202 (bit-wise select) are compared with the eleven bits of state machine input bus 1110 by comparator 1214. OR gate 1218 is used to mask the output bits of comparator 1214 with the contents of

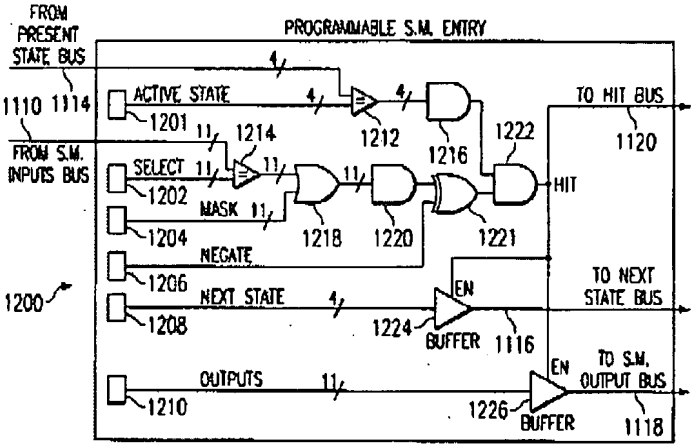

FIG. 12

storage element 1204 (bit-wise mask). The results of this masking operation are ANDed together using AND gate 1220, resulting in a match result for the state machine input bus. Exclusive OR gate 1221 couples the output of AND gate 1220 to one of the inputs of AND gate 1222 as shown, and also provides a selectable inversion function. That is, when negate bit 1206 is set to "0," the output of exclusive OR gate 1221 follows the output of AND gate 1220; but when negate bit 1206 is set to "1," the output of exclusive OR gate 1221 is the opposite of the output of AND gate 1220. The match results for present state and for the state machine input bus are ANDed together by AND gate 1222 to produce the HIT signal, which is coupled to HIT bus 1120.

In the circuitry described above, if only one of the selected bits of the state machine input bus is set, AND gate 1220 will not reflect a match. There is no teaching or suggestion in *Ranson* of activating an increment signal when one or more selected bits are set; the only provision in *Ranson* is for activating an increment signal when all of the selected bits are set.

Based on the foregoing, Applicant respectfully submits that the base claims 1, 16 and 27 are not anticipated or suggested by

the applied art of record, and are therefore in condition for allowance. Claims 2-15 depend from base claim 1, claims 17-26 depend from claim 16, and claims 28-36 depend from base claim 27; each of the dependent claims introducing additional limitations therein. Accordingly, these dependent claims are also believed to be allowable.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims and in further view of the above remarks and/or amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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